IN THE CLAIMS

1 (Original). A method comprising:

receiving a data frame of a first size;

demultiplexing said data frame;

writing blocks of the demultiplexed data frame at the first size into a register;

reading blocks of a second size, different from said first size, from said register; and

multiplexing said blocks to form an output data frame of the second size.

2 (Original). The method of claim 1 wherein receiving a data frame of a first size includes receiving a 64-bit data frame.

3 (Original). The method of claim 2 wherein demultiplexing said data frame includes providing said data frame to a one to thirty-three demultiplexer.

4 (Original). The method of claim 3 wherein writing blocks of the demultiplexed data frame at the first size includes writing blocks of 64-bits to a register.

5 (Original). The method of claim 4 wherein writing the blocks into a register include writing 2,112 bits into a register.

6 (Original). The method of claim 5 including controlling a write pointer at a frequency of approximately 161 MegaHertz.

7 (Original). The method of claim 5 wherein reading blocks of the second size includes reading blocks of sixty-six bits from said register.

8 (Original). The method of claim 7 including controlling a read pointer at a frequency of approximately 156 MegaHertz.

9 (Original). The method of claim 7 wherein multiplexing said blocks to form an output data frame of a second size includes forming an output data frame by using a thirty-two to one multiplexer.

10 (Original). The method of claim 1 including converting a sixty-four bit data frame to a sixty-six bit data frame.

11 (Original). A device comprising:

a demultiplexer coupled to receive a data frame of a first size;

a register coupled to receive data from said demultiplexer; and

a multiplexer coupled to the output of said register, the output of said multiplexer being a data frame of a second size different from said first size.

12 (Original). The device of claim 11 including a first counter to control the writing of data from said demultiplexer to said register.

13 (Original). The device of claim 11 including a second counter to control the reading of data from said register to said multiplexer.

14 (Original). The device of claim 11 wherein data is written to said register at approximately 161 MegaHertz and data is read from said multiplexer at approximately 156 MegaHertz.

15 (Original). The device of claim 11 wherein said demultiplexer receives a data frame of 64-bits and said multiplexer outputs a data frame of 66-bits.

16 (Original). The device of claim 11 wherein said demultiplexer is a one to thirty-three demultiplexer.

17 (Original). The device of claim 11 wherein said multiplexer is a thirty-two to one multiplexer.

18 (Original). The device of claim 11 wherein said demultiplexer writes data to said register in 64-bit blocks.

19 (Original). The device of claim 11 wherein said multiplexer reads data from said register in 66-bit blocks.

20 (Original). The device of claim 11 wherein said demultiplexer writes data in blocks of a first size to said register and said multiplexer reads data in blocks of a second size, different from said first size, from said register.

21 (Original). The device of claim 11 wherein said device is part of a physical coding sublayer.

22 (Original). The device of claim 21 wherein said device is part of a receiver in a fiber optic network.

23 (Original). A method comprising:

receiving a stream of data;

defining a window of a predetermined size within said stream;

examining the window to determine whether at least one synchronization bit is located within the data in the window; and

shifting the window along said stream if a valid synchronization bit is not found in the window.

24 (Original). The method of claim 23 including shifting the window by a predetermined number of bits and filling the opening created by shifting with a bit from a previous cycle.

25 (Original). The method of claim 24 including storing bits from each successive cycle and providing bits from previous cycles to fill openings created by shifting in subsequent cycles.

26 (Original). The method of claim 23 including successively shifting said window by one bit along said stream of data until valid synchronization bits are located.

27 (Original). The method of claim 23 including locating a pair of synchronization bits in a 66-bit data frame.

28 (Original). The method of claim 23 including receiving a block of data of said predetermined size in a multiplexer and multiplexing said data into a register.

29 (Original). The method of claim 28 including applying two of said bits from said register to an exclusive OR gate.

30 (Original). The method of claim 23 including providing 66-bit blocks in successively shifted sets, each block shifted one-bit relative to the other block, to a multiplexer and successively applying said 66-bit blocks to a register.

31 (Original). The method of claim 23 including providing serial data to a first array of multiplexers arranged in rows and columns, wherein each row corresponds to a different window position along the stream of data.

32 (Original). The method of claim 31 including writing the data from a row of multiplexers in a first array to an array of multiplexers in a second array.

33 (Original). A device comprising:

a first storage element to receive a stream of data;

an element to define a window of a predetermined size within said stream;

a detector to examine the window to determine whether at least one synchronization bit is located within the data in the window; and

a component to shift data along said stream into said window if a valid synchronization bit is not found in the window.

34 (Original). The device of claim 33 including:

a multiplexer coupled to said data stream and said first storage element to receive data;

a second storage element coupled to the output of said multiplexer to receive a data frame;

a gate coupled to said second storage element to test for the presence of at least one synchronization bit in said data frame in said second storage element; and

a control to determine whether or not valid synchronization bits have been located in a series of data frames.

35 (Original). The device of claim 34 wherein said control is a state machine.

36 (Original). The device of claim 35 including a counter, wherein said state machine controls the counter that controls the operation of said multiplexer.

37 (Original). The device of claim 34 wherein said first and second registers are sixty-six bit registers.

Claims 38 and 39 (Canceled).

40 (Original). The device of claim 34 wherein said gate is an exclusive OR gate.

41 (Original). The device of claim 40 wherein said exclusive OR gate tests two bits of each data frame for the presence of synchronization bits.

42 (Original). The device of claim 34 wherein said first storage element stores bits from each successive cycle and provides bits from previous cycles to fill openings created by shifting in subsequent cycles.

43 (Original). The device of claim 42 including a counter that receives a signal from said control and issues a signal to said multiplexer to shift a window of data output by said multiplexer along said serial data stream.

44 (Original). The device of claim 33 wherein said first storage element includes an array of multiplexers arranged in rows and columns.

45 (Original). The device of claim 44 wherein each row of multiplexers provides one window of data.

46 (Original). The device of claim 45 including a second array of multiplexers coupled to said first array of multiplexers.

47 (Original). The device of claim 46 including a register that receives the output from said second array of multiplexers.

48 (Original). The device of claim 47 including a gate to determine whether or not at least one bit in said register is a synchronization bit.

49 (Original). The device of claim 48 including a state machine coupled to the output of said gate.

50 (Original). The device of claim 49 wherein said gate is an exclusive OR gate.

51 (Original). The device of claim 49 including a state machine coupled to the output of said gate.

52 (Original). The device of claim 51 including a counter coupled to said state machine and said first array of multiplexers to select a row of multiplexers in said first array.

53 (Original). The device of claim 51 including a gear box to convert 64-bit data frames to 66-bit data frames.

54 (Original). The device of claim 53 further including a physical coding sublayer.

55 (Original). The device of claim 54 where said device is a receiver for a fiber optic network.